REMARKS

Claims 1-5 and 7-20 are pending in the present application. Replacement claims 1, 9, 12 and 15 are presented herewith. Claim 6 has been canceled.

Priority Under 35 U.S.C. 119

Applicants note the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119 and receipt of the certified copy of the priority document.

Drawings

Applicants acknowledge receipt of the Notice of Draftsperson's Patent Drawing Review form PTO-948 and that the drawings have been objected to as having characters and lines that are not uniformly thick and well defined. Corrected formal drawings will be prepared and filed in due course upon indication of allowance of the present application.

Claim Objections

Claim 6 has been objected to under 37 C.F.R. §1.75(c) as being of improper dependent form, for failing to further limit the subject matter of a previous claim. Although Applicants do not necessarily concede that this objection is proper, claim 6 has been canceled to expedite prosecution of this application. The Examiner is therefore respectfully requested to withdraw this objection.

Claim Rejections-35 U.S.C. 102

Claims 1-5, 8 and 11 have been rejected under 35 U.S.C. 102(e) as being clearly anticipated by the Al-Shareef et al. reference (U.S. Patent No. 6,162,744). This rejection, insofar as it may pertain to the presently pending claims, is traversed for reasons that will follow.

Claim Rejections-35 U.S.C. 103

Claims 6, 7 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Al-Shareef et al. reference. This rejection is respectfully traversed for the following reasons.

The method for manufacturing a capacitor of a semiconductor device of claim 1 includes in combination "performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature", and "performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature". As featured, the first and second post-annealings are performed in-situ. Applicants respectfully submit that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

The Examiner has alleged that the annealing conditions as claimed are well known and can be performed either separately or in-situ. However, Applicants respectfully emphasize that in-situ annealing as featured in claim 1 has the advantage of simplifying the semiconductor manufacturing process, thus to reduce manufacturing

expenses and to increase throughput. The Al-Shareef et al. reference as relied upon by the Examiner does not disclose or even remotely suggest performing the first and second annealings in-situ, and particularly not in consideration of the above-noted advantages. The first and second annealings are described in general in column 4, lines 17-67 of the Al-Shareef et al. reference, and there is no disclosure or suggestion that these annealings are in-situ.

In absence of at least a suggestion of in-situ annealing in the relied upon prior art, Applicants respectfully submit that the Examiner has relied upon impermissible hindsight to maintain this rejection. Applicants therefore respectfully submit that claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection, insofar as it may pertain to any of claims 1-5, 7, 8, 10, 11, 13 and 14, is improper for at least these reasons.

Claims 9, 10, 12, 13 and 15-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Al-Shareef et al. reference, in further view of the Azuma et al. reference (WO 96/02067) and the Wolf et al. article (Silicon Processing for the VLSI Era). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Claim 9 has been amended to be in independent form. Particularly, the method for manufacturing a capacitor of a semiconductor device includes in combination performing the first and second post-annealings after forming of the plate electrode. Applicants respectfully submit that the prior art as relied upon by the Examiner does not disclose or suggest these features.

The Examiner has alleged on page 4 of the Office Action dated April 11, 2001, that the Al-Shareef et al. reference anticipates performing one or both anneals after the formation of the second electrode, and has directed attention to column 5, lines 6-10 as support thereof. However, as described beginning in column 4, line 17 of the Al-Shareef et al. reference with respect to Fig. 2, substrate 10 and dielectric layer 26 are subjected to a first annealing. As subsequently described beginning in column 4, line 40 with respect to Fig. 2, after the first annealing, the substrate and the dielectric layer 26 are then subjected to a second annealing. As still further described beginning on column 5, line 1 of the Al-Shareef et al. reference with respect to Fig. 3, the diffusion barrier layer 28 is subsequently formed over layer 26, and a second capacitor electrode layer 30 is formed over layer 28 and also over capacitor dielectric layer 26. The second capacitor electrode layer 30 is then patterned to produce a second capacitor electrode 32, as illustrated in Fig. 4. As specifically disclosed in column 5, lines 6-8 of the Al-Shareef et al. reference, the subject annealings are conducted **prior to formation of any portion of second capacitor electrode 32.**

Accordingly, as may be readily understood in view of the above noted portions of the Al-Shareef et al. reference, the first and second annealings are conducted **prior to formation** of the second capacitor electrode 32. Contrary to the Examiner's assertion, the Al-Shareef et al. reference does not disclose or even remotely suggest first and second post-annealings being performed **after forming of a plate electrode**, as featured in claim 9.

The Examiner has asserted that it would have been obvious to anticipate the process of performing both first and second annealings after formation of the plate electrode or the interdielectric, in view of the combined prior art. The Examiner has asserted that one would have been motivated in order to avoid the risk of oxidation of the electrodes from out-diffusion of oxygen from the high dielectric layer. However, as should be clear from the above comments, the Al-Shareef et al. reference in column 5, lines 6-11 actually teaches away from annealing after formation of a plate electrode or interdielectric, as suggested by the Examiner. Particularly, the Al-Shareef et al. reference teaches performing the annealings **prior to formation** of the second capacitor electrode 32 to reduce oxidation from out-diffusion. It should also be noted that as emphasized on page 11, lines 4-7 of the present application, post-annealing after formation of the plate electrode has the advantage of providing high capacitance and low leakage characteristics, whereby oxidation of the barrier layer is suppressed.

With regard to the Azuma et al. reference, the first anneal in step P47 of Fig. 4 is performed **prior to** depositing the second electrode in step P48. Accordingly, the Azuma et al. reference as relied upon by the Examiner does not disclose or suggest first and second post-annealings performed after formation of a plate electrode. With regard to the Wolf reference, it is not understood how Table 4 on page 57 may be interpreted as disclosing or suggesting the concept of performing first and second post-annealings after formation of a plate electrode, as featured in claim 9.

Accordingly, Applicants respectfully submit that the method for manufacturing a

capacitor of a semiconductor device of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claim 9, is improper for at least these reasons. Applicants also respectfully submit that the method for manufacturing a capacitor of a semiconductor device of claim 15 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 15-20, is improper for at least similar reasons.

Claim 12 has been amended to be in independent form. The method for manufacturing a capacitor of a semiconductor device of claim 12 includes in combination first and second post-annealings that are performed after forming of the interdielectric layer. In greater detail, the interdielectric layer is formed over the plate electrode. The first and second post-annealings are performed after forming the interdielectric layer on the plate electrode. As emphasized previously, the prior art as relied upon by the Examiner does not disclose or even remotely suggest performing first and second post-annealings after formation of a plate electrode. The prior art thus clearly fails to disclose or even remotely suggest performing first and second post-annealings after an interdielectric layer has been formed on a plate electrode. Accordingly, Applicants respectfully submit that the method for manufacturing a capacitor of a semiconductor device of claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claim 12, is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections and to pass the claims of the present application to issue for at least the above reasons. Applicants also respectfully emphasize that claim 1 has been amended to include the features of dependent claim 6, and claims 9 and 12 have been amended to be in independent form. As such, these amendments should not be construed as limiting scope within the meaning of *Festo*.

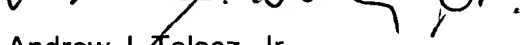
In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of one (1) month to August 11, 2001, for the period in which to file a response to the outstanding Office Action. The required fee is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

JONES VOLENTINE, P.L.L.C.



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Enclosures: Version with marked-up changes

SEC.506

What is claimed is:

(Amended)

1. A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode over the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature.

) IP the first and second post-annealings being performed in-situ

2. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the high dielectric layer comprises a material selected from the group consisting of $(Sr, Ti)O_3$, $(Ba, Sr)TiO_3$, $Pb(Zr, Ti)O_3$, and $(Pb, La)(ZrTi)O_3$.

3. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the plate electrode and the storage electrode comprises a material selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

4. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first temperature is between 600°C and 900°C.

5. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the second temperature is between 100°C and 600°C.

6. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed separately or in-situ.

7. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed in a furnace or a rapid vacuum thermal annealing apparatus.

8. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed after the step of forming the high dielectric layer.

(Amended)

9. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed after the step of forming the plate electrode.

comprising: forming a storage electrode over a semiconductor substrate; forming a high dielectric layer over the storage electrode; forming a plate electrode over the high dielectric layer; performing a first post-annealing of the semiconductor substrate under an inert atmosphere; and performing a second post-annealing of the semiconductor substrate, after the first post annealing, at a second temperature lower than the first temperature.

SEC.506 storage electrode; ☞ forming a plate electrode over the high dielectric layer; ☞ performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; ☞ performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature; and ☞ forming an interdielectric layer over the plate electrode,

10. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

11. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising forming an interdielectric layer over the plate electrode.

(Amended)

12. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 11, wherein ☞ the first and second post-annealing steps are performed after the step of forming the interdielectric layer.

13. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 11, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

14. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising performing a third post-annealing, after the second post-annealing, at a third temperature lower than the second temperature.

(Amended)

15. A method for manufacturing a capacitor of a semiconductor device in which a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer are sequentially formed on a semiconductor substrate, further comprising:

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature, after forming one of the high dielectric layer, the plate electrode, and the interdielectric layer; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature.

IP the first and second post-annealings being performed after forming of the plate electrode

16. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the high dielectric layer comprises a material selected from the group consisting of (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3, and (Pb, La)(ZrTi)O_3.

17. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the plate electrode and the storage electrode comprise a material selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

18. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the first temperature is between 600°C and 900°C.

Abstract of the Disclosure

A method ~~is provided for~~ of manufacturing a capacitor ~~of a semiconductor device in~~ includes sequentially forming ~~which~~ a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer ~~are sequentially formed~~ over a semiconductor substrate. ~~This method includes the steps of performing~~ a first post-annealing of the semiconductor substrate is performed under an inert atmosphere at a first temperature, and then ~~performing~~ a second post-annealing is performed ~~of the semiconductor substrate~~ at a second temperature. The first and second post annealings ~~steps~~ can be performed after forming ~~the deposition of~~ the high dielectric layer, the plate electrode, or the interdielectric layer, or any combination thereof, ~~of this, so~~ long as the second post-annealing step is performed after the first post-annealing step. The two post-annealings ~~steps do not have to be~~ are not necessarily performed in the same place or ~~at the same~~ stage ~~during the fabrication process~~. The first temperature may be ~~is preferably in the range of~~ about 600°C to 900°C, and the second temperature ~~is preferably in the range of~~ about 100°C to 600°C. ~~In this way,~~ As a result, the dielectric constant of the high dielectric layer is increased, and the leakage current is reduced.